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Logic Gates Realization using Spiking Neural Network and Vedic Maths - A Comprehensive Study

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Abstract—*Logic gates like AND, OR, NOT gate etc are the basic component in the digital circuit and it is just like heart beat and blood of the digital electronics. In every small digital circuit logic gates are used. Functioning of logic gate can be improved by using artificial spiking neural network. A spiking neural network is a massively parallel distributed processor and it is much better than perceptron neural network. It has a natural propensity for storing experiential knowledge and making it available for use, and due to this they are useful in applications like pattern recognition, robotics, prediction problems, system identification, and control problems. Boolean logic realization using artificial spiking neural network are known as Neuronal Logic.*

ANN models require simple and low precision computations which can performed parallel functioning and hence faster. This can be implemented on cheap and low precision hardware. Basic Neural network involves enormous number of multiplication and addition calculations. It has been already proved that multipliers based on Vedic mathematics are much faster in speed than the standard multipliers. In the present study, we have explored the possibility of hardware realization of spiking neuronal logic gates using Vedic multipliers herein referred to as Vedic neuron. This is achieved by performing the spiking neural network computations using Vedic mathematics rather than the conventional multiplication process. The multiplier is based on the 'UrdhvaTiryagbhyam' sutra, which is one out of sixteen sutras of ancient Vedic mathematics. Basic logic gates like AND, OR and AND-NOT have been studied and its hardware implementation using neural network has been theoretically worked out. A comprehensive study was carried out on the computation speed of neuronal logic gates implemented using standard multipliers as well as neuronal logic gates implemented using Vedic multipliers. The increase in processing speed with Vedic neuron implementation can be of use in several real time operations where speed is critical.

Keywords*: Spiking neural network; Vedic multiplier; Urdhva Tiryagbhyam; Neuronal Logic.*

1. INTRODUCTION

Logic gates and circuits plays a major role in the theory of implementation, computation, and optimal structure for classical logic circuits have been developed. Computation-whether by man or by machine-is a physical activity, and is ultimately governed by physical principles. A very important role for mathematical theories of computation is to reduce in their axioms, in some different way. With this support, the focus can be on the abstract modeling of complex computing processes without having to verify at every step the physical reliability of the model [1]. Thus, a Boolean logic (using, say, the AND, NOT, and OR primitives) with the confidence that any network designs in this way is immediately translatable in to a working circuit requiring only well-understood, readily available components (the "gates," "inverters," and "buffers" of any suitable digital-logic family).

The human brain, which consists of approximately 100 billion neurons that are connected by about in trillions of connections, which forms the most complex object known in the whole universe. Brain functions such as sensory information processing with the help of motor neuron and cognition are the results of emergent computations carried out by this massive network of neurons. The Spiking neural networks are used for a number of applications including such as it is used in image processing, identification and recognition, classification, GPS systems, speech, vision, and control systems [2-4]. They can be also trained to solve things that are difficult for conventional computers or human beings. Additionally, they have attractive properties like adaptiveness, self-organization, nonlinear network processing and parallel processing. This has lead to the use of neural network in applications involving association, classifications and decision-making and reasoning [5]. Artificial neural networks consist of massively parallel network and require parallel architecture for high speed operations in real time applications [6].

Multiplier is a crucial block in designing arithmetic, signal and image processors; such high speed multipliers play an important role in designing an efficient architecture [7, 8]. Recently, several high speed multipliers designed using Vedic mathematics have been reported [9, 10]. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics into very simple one and reduces the computation time. This is because the Vedic formulae are claimed to be based on the natural principles on

which the human mind works. Vedic mathematics is a collection of arithmetic rules that allow more efficient speed implementation.

Hardware realization of logic gates using Spiking Neural Network is known as Neuronal Logic. This depends on the efficient implementation of a single neuron. Reconfigurable computing architectures based on FPGAs are suitable for hardware implementation of neural networks. Challenging task is the FPGA realization of SNNs with a large number of neurons[11].

In this paper, features of SNN & Vedic multiplier are studied for the hardware realization of logic gates to theoretically estimate the performance of logic gates implemented using standard neuron as well as logic gates implemented using Vedic neuron. Also, the hardware implications of both the schemes have been studied. Section II presents a brief introduction about ANN. Section III gives an explanation of Vedic multiplier with UrdhvaTiryagbhyam sutra. Section IV explains about the design and hardware implementation of the proposed work. Section V explains the theoretical results of the study. The last section VI deals with the conclusion of the comprehensive study.

2. ARTIFICIAL NEURAL NETWORKS

The work on artificial network has been motivated from the working of human brain in a way that brain is a highly complex nonlinear and parallel computer with a capability to organize its structural constituents known as neurons so as to perform the certain computation many times faster than that of the digital hardware [4]. Artificial neural networks are computational models which are inspired by the principles of computations performed by the biological neural networks of the brain. Neural networks possess many attractive characteristics that may ultimately surpass some of the limitations in classical computational systems. The computation can be viewed as a system in which the inputs are received from an external stimulus. The receptors convert the external stimulus into electrical impulses that convey the information to the neural net and depending on the electrical impulses the neural net conveys or transmits the information to effectors to provide an optimal response to stimulus as shown in “Fig.1”. Neuron is the integral constituent of brain composition. The brain learns to distinguish different patterns by training these neurons which give the appropriate output [11].

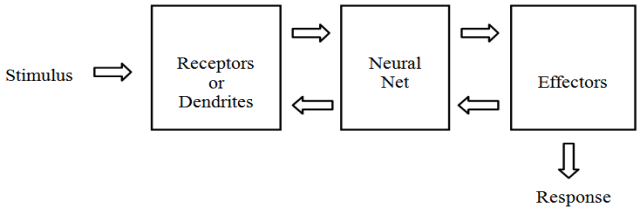

Fig. 1: Block Diagram of Nervous system

The concept of artificial neural network has been designed to model the way in which the brain performs a particular task or function of interest.

A neural network is a massively parallel distributed network made up of simple processing units, which has a

natural tendency of storing experiential knowledge and making it available for use [12]. It is analogous to the brain in two aspects:

- The network obtains knowledge from its environment through a learning process.
- Interneuron connection strengths which is known as synaptic weights store the acquired knowledge.

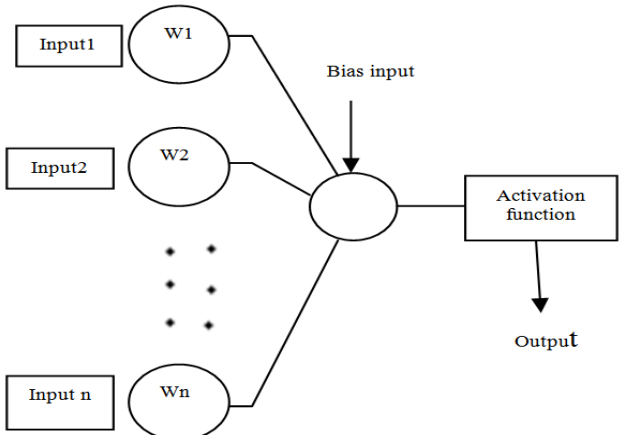

Fig. 2: Nonlinear model of Neuron [5]

3. SPIKING NEURAL NETWORKS

Spiking neural network comes under the third generation neural network models. It increases the level of realism in a neural simulation. In addition to synaptic state.SNN also incorporates the concepts of time in their operating model.

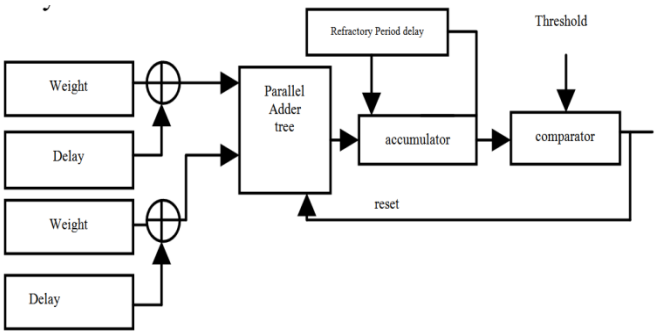

Fig. 3: Block Diagram of a Single Neuron

The idea of neuron in the SNN does not fire at each propagation cycle as it happens in perceptron neural network models but rather fire only when its membrane potential reaches to some specific value. When neurons fires signal is

generated and travel to other neurons which increases or decreases the potential according with the signal. In Spiking neural network the current activation level considered to be the neuronal state with incoming of spikes pushing this in higher values then it will either fire or decay.

4. INTRODUCTION TO MULTIPLIER

Multiplication is an essential and basic function in arithmetic procedures and Vedic mathematics is an ancient methodology developed by Indians, which is capable of faster intellectual computation. Multiplication is one of the most important operations in digital neural network based systems. There are several Multiplication-based operations. Frequently used such Computation- Intensive Arithmetic Functions are multiply and Accumulate (MAC) and inner product [20]. Further, multipliers play a major role in the overall power consumption of any system. Therefore, reducing their power dissipation satisfies the overall power budget of ANN system.

Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [21]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. The essential requirements for many applications developed using neural network are reduction of the time delay and power consumption.

4.1 Vedic Multiplier

The word “Vedic” which was used in epic period is a Sanskrit word derived from the word, ‘Veda’ which means knowledge. When it is applied to scripture, it signifies a book of knowledge. According to the Tirthaji, all of Vedic mathematics is based on 16 sutras, or word formulae. It is a unique technique of calculations based on simple principle and rules with which any mathematical problem like arithmetic, algebra, trigonometry can be solved mentally. In Vedic mathematics, is said to manifest the coherent and unified structure of arithmetic, and its methods are complementary, direct and easy [22, 23]. In Vedic mathematics, Urdhva Tiryagbhyam sutra which means vertically and crosswise is used generally for high speed multiplication. Vedic multiplier is very much advantageous in case of bigger multiplication which would consume more time as compared to other multiplier.

4.2 Details of Urdhva-Tiryagbhyam Method of Multiplication

UrdhvaTiryagbhyam sutra is a sutra for multiplication in the epic Indian Vedic mathematics. This is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. This is based on the generation of all partial products by means of concurrent addition of the partial product. UrdhvaTiryagbhyam obtains parallelism in multiplication. Vedic mathematics reduces the typical calculations in conventional mathematics into very simple one. This sutra uses Vedic formulae that are based on the natural principles written by Tirthaji on which the human brain works. Vedic mathematics is a technique of arithmetic rules that perform high speed computation. UrdhvaTiryagbhyam is a basic sutra applicable to all cases of multiplication.

4.3 Urdhva Multiplier Hardware Architecture

The 'UrdhvaTiryagbhyam' algorithm can be implemented for binary number system in the same way as decimal number system. As an example, a 4x4 Vedic multiplier hardware implementation is explained.

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules. Let’s examine 4x4 multiplication say a=dcba and b=DCBA. The output for the multiplication result is $s_7s_6s_5s_4$ $s_3s_2s_1s_0$. Divide a and b into two parts say dc & ba for a and DC & BA for b using the fundamentals of Vedic multiplication, by taking two bits at a time and using 2 bit multiplier block.

The structure for multiplication will be as shown in “Fig. 4”. Each block, as shown is a 2x2 bit Vedic multiplier. The inputs to the first multiplier are ba and BA. The last block is a 2x2 bit multiplier with inputs dc and DC.

The middle one shows two 2x2 bit multipliers with inputs dc & BA and ba & DC. The final result of multiplication is of 8 bits, $s_7s_6s_5s_4$ $s_3s_2s_1s_0$. To get final product ($s_7s_6s_5s_4$ $s_3s_2s_1s_0$) four 2x2 bit Vedic multiplier and three 4-bit Ripple-Carry (RC) adders are required.

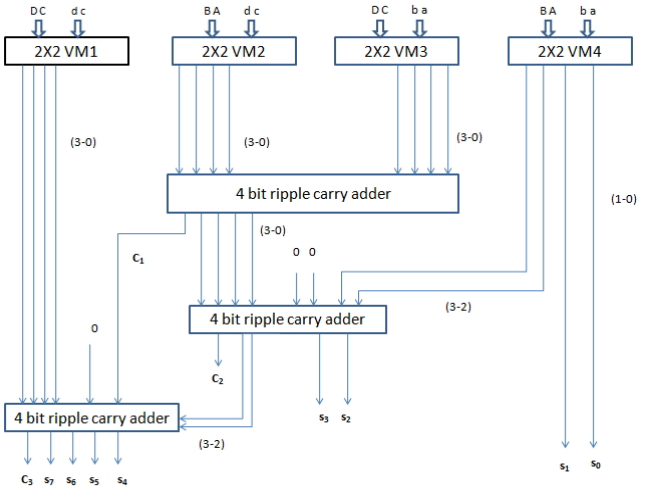

Fig. 4: Block Diagram of 4x4 bit Vedic Multiplier

5. NEURONAL LOGIC

The brain is composed of Boolean entities functioning as threshold units. These simplified units constitute pure and reliable logic-gates (e.g., AND, XOR), similar to the logic at the core of computers. Generalization of this simplified

Boolean framework to include unreliable elements has emerged in 1956 by the innovative work of John von Neumann. The Von Neumann concepts as well as the earlier pioneering work of Claude Shannon to simplify Boolean circuits (Shannon, 1938) are at the cornerstone of the present day's computational paradigm (Turing, 1938) [24].

Using the spiking neuronal logic model we can model logic functions. Below figure Fig.5 shows and describes the architecture for three logic functions – AND, OR & AND-NOT.

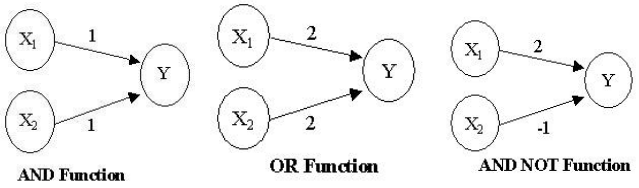

Fig. 5: Neuronal Logic Gates

The truth tables for each function are also shown in table I.

Table 1: Truth table for and,or & and-not logic gates

AND		
X_1	X_2	Y
1	1	1
1	0	0
0	1	0
0	0	0

OR		
X_1	X_2	Y
1	1	1
1	0	1
0	1	1
0	0	0

AND NOT		
X_1	X_2	Y
1	1	0
1	0	1
0	1	0
0	0	0

Fig. 6: Vedic neuron Architecture

A) AND Function

Since X_1 and X_2 inputs are connected to the same neuron the connections must be the same. In the above case this is 1. For modeling the AND function the threshold on Y shall be set to two (2).

B) OR Function

OR function is similar to the AND function except the connections are set to 2. The threshold value on Y is also set to two (2).

C) AND NOT Function

The AND-NOT function is not symmetric in that an input of 1,0 shall be treated in a different way to an input of 0,1. It is clear from the truth table that 'true' (value of one) is returned is when the first input is true and the second input is false. Again, the threshold on Y is set to 2.

6. ARCHITECTURE OF VEDIC NEURON

The proposed hardware of a Vedic neuron is almost similar to a standard non-linear neuron (spiking neural network model) except for the multiplier. The standard multiplier is replaced with a Vedic multiplier which multiplies the inputs with weights. For evaluation purpose the weights were randomly fixed. The architecture of a single neuron as shown is fig.6, which has been designed using Vedic multiplier instead of standard multiplier, to achieve higher speed in designing neural nets. Neuronal logic gates can be implemented using this architecture.

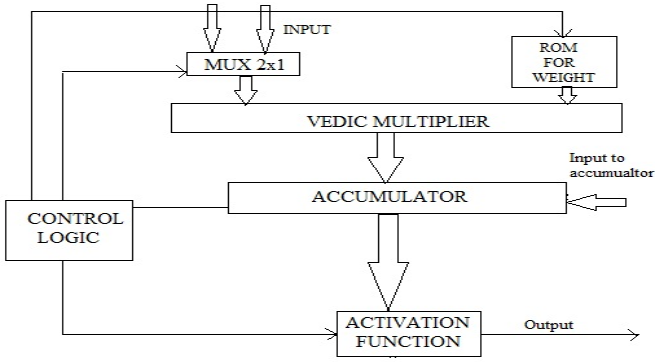

Fig. 6: Vedic neuron Architecture

7. THEORETICAL RESULTS

From [25], it can be found that the 4*4 multiplier by Kabiraj Sethi has a delay of 17.45ns and the Vedic multiplier has a delay of 11.695ns. Also, it has been proved in that the Vedic multiplier is faster than standard multiplier in [21, 22, and 23].

With the application of Vedic multiplier, the above latency of neuronal logic can be bought down to an appreciable amount. This can be of great use in applications where speed is very critical.

8. CONCLUSIONS

The technologies like SNN & Vedic mathematics (multiplier) are the two important and promising technologies which can increase the processing speed. In this paper, a comprehensive study to combine these two technologies to achieve a high performance neuronal logic gates which can be utilized in various fields where computational speed is the main concern. The results of Boolean logic gate using standard and Vedic neuron have been explored. Hence, the comparison result from various papers indicates that Vedic multiplier is faster than standard multipliers.

Also, this comprehensive study can be practically verified by means of hardware implementation in FPGA and verifying the speeds of neuronal logic gates with Vedic multipliers.

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